REMARKS

The Office Action dated June 11, 2003, has been received and carefully noted. The following remarks are submitted as a full and complete response thereto. In view of the following remarks, Applicants request the favorable consideration of claims 1-8.

Claims 3, 4, and 6-8 were rejected under 35 U.S.C. § 112, first paragraph as containing subject matter which is not described in the specification in such a way as to enable one skilled in the art to make or use the invention. The Office Action states that the feature of "adjusting of said delay is irrespective of said comparison when starting the step of adjusting of said delay" as recited in claims 3, 4, 6, and 7 is not described in the specification. Applicants respectfully disagree. Applicants submit that the specification clearly recites the features of the claimed invention.

The claimed invention provides the benefit of providing a delay time adjusting circuit and a delay time adjusting method, which can easily adjust a delay time of a signal even when the signal has a high frequency. Figure 5 illustrates the features of an input buffer 1, the output buffer 5, the frequency dividers 2 and 4, a DLL array 7, dummy circuit 6, the phase comparator 8, a delay adjuster 24, a state judgment circuit 20, and a state detection circuit 22. These features and there functions are clearly described in the specification.

The Office Action takes the position that the feature of the recited feature of "adjusting of said delay is irrespective of said comparison when starting the step of adjusting of said delay" as recited in claims 3, 4, 6, and 7 is not described in the specification. Contrary to the Examiner's position, the state detection circuit 22 and the state judgment circuit 20 as described in the specification on pages 19-22 and illustrated in Figures 11-12 clearly enable and distinctly recite the features and functions of the claimed invention.

The state detection circuit 22 comprises a delay circuit 40, inverters 41 to 45, a NOR circuit NOR1, gates GT1 and GT2, N-channel MOS transistors NT1 to NT7, and P-channel MOS transistors PT1 to PT8. The delay circuit 40 includes serially connected inverters 46 to 48 and MOS capacitor MC1 and MC2. (See Page 19, Lines 8-14). The following description is not new matter and more clearly describes the operation of claimed invention as illustrated in Figures 11 and 12.

Initially, if the signal "out" is "H" when the signal "resz" is generated, the outputs (N3,

N4) of the inverters 43 and 44 are set to "L" due to the generation of the signal "resz". Accordingly, the signal "fstz" is set to "H", which results in the signal "upz" being set to "H". At this time, the gate GT1 is disconnected. Next, when the signal "out" changes from "H" to "L", an "H" pulse is generated at the output (N2) of the NOR1, and the gate GT1 is connected, and subsequently, the gate GT2 is connected. Thus, the state of the inverter 43 is transferred to the signal "fstz", which results in the signal "fstz" being set to "L". After the signal "fstz" is set to "L", the signal "fstz" is fixed to "L". Since the output of the inverter 43 does not invert once set to "1", the signal "fstz" is maintained at "L" even if the "H" pulse is generated many times. After the signal "fstz" is set to "L", the signal "upz" changes in accordance with the signal "out".

Next, if the signal "out" is "L" when the signal "resz" is generated, the outputs (N3, N4) of the inverters 43 and 44 are set to "L" due to the generation of the signal "resz". Accordingly, the signal "fstz" is set to "H", which results in the signal "upz" being set to "H". At this time, the gate GT1 is disconnected. Subsequently, if the signal "out" changes from "L" to "H", the gate GTI maintains the disconnected state since no pulse is generated at the output (N2) of the NORI. Additionally, the signal "fstz" maintains at "H" since the state of the inverter 43 is not transferred to the signal "fstz". Then, when the signal "out" changes form "H" to "L", an "H" pulse is generated at the output (N2) of the inverter 43, which results in connection of the gate GT2. Accordingly, the state of the inverter 43 is transferred to the signal "fstz" and the signal "fstz" is set to "L". After that, the signal "fstz" is fixed to "L".

As a result, when the signal "resz" is generated, the signal "upz" is set to "H" whether the signal "out" is "H" or "L" (irrespective of the level of the "out" signal), which results in gradual increase in the delay. However, if the signal "out" is "H" when the signal "resz" is generated, the signal "upz" is set to "L" in response to the first change of the signal "out" from "H" to "L". After that, the signal "upz" changes in response to the value of the signal "out", which results in a decrease or increase in the delay in response to the value of the signal "out". Finally, if the signal "out" is "L" when the signal "resz" is generated, the first change of the signal "out" from "L" to "H" is ignored and the signal "upz'' is set to "L" in response to the second change of the signal "out" from "H" to "L". After that, the signal "upz" changes in response to the value of the signal "out", which results in decrease or increase in the delay in response to the value of the signal "out". (See Pages 19-23 and

Figures 11 and 12). As a result, the adjusting of the delay is irrespective of the comparison when starting the step of adjusting of the delay. In view of the above description of Figures 11 and 12, Applicants respectfully requests the withdrawal of the rejection of claims 3, 4 and 6-8 under 35 U.S.C. 112, first paragraph.

Claims 3, 4, and 6-8 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Applicants respectfully submit that in view of the above description as supported in the specification and drawings as originally filed, the features of the present invention are clearly and distinctly recited in claims 3, 4, and 6-8. Specifically, the feature of adjusting of the delay is irrespective of the comparison when starting the step of adjusting of the delay, is clear and definite, as recited in claims 3, 4, and 6-8. Therefore, Applicants respectfully request the withdrawal of the rejection of claims 3, 4, and 6-8 under 35 U.S.C. 112, second paragraph.

Claims 1 and 2 were rejected under 35 U.S.C. § 102(b) as being anticipated by Applicant's Admitted Prior Art. The Examiner takes the position that the Admitted Prior Art (APA) teaches or suggests all the features recited in claims 1 and 2. Applicants respectfully disagree.

Claim 1 is directed to a delay time adjusting method of adjusting a delay time of an input signal so that a phase of the input signal and a phase of an output signal match each other, based on a comparison between phases of the input signal and the output signal. The method comprises the step of increasing the delay time in response to a signal, which indicates a start of adjusting the delay time to adjust the phase of the output signal.

Figure 1 discloses a conventional delay time adjusting circuit. The convention delay time adjusting circuit comprises an input buffer, an output buffer, frequency dividers, a DLL array, a dummy circuit, a phase comparator, and a delay adjuster. The delay adjuster supplies a control signal CS to the DLL array. The Office Action interprets that the signal CS shown in FIG.1 corresponds to the signal, which indicates a start of adjusting the delay time. Applicants respectfully disagree with this interpretation.

Contrary the Office Action's position, the control signal CS is not a signal which indicates a start of the adjustment of the delay time but a signal indicating a setting value of the delay time. In FIG. 1, it is determined first whether the delay is to be increased or decreased by comparing the target clock signal "tclk" with the delay clock signal "dclk" by

the phase comparator B. Then, the delay adjuster 10 determines the setting value of the DLL array in accordance with the determination of increase or decrease of the delay. The determined setting value is sent to the DLL array as the control signal CS.

The DLL array 3 in FIG. 1 has inverters connected in series as shown in FIG. 2. Thus, the delay time can be set by connecting one of the switches provided to the respective inverters. The DLL array changes the delay time in response to the signal CS. In other words, the signal CS is used for selecting one of the switches. The delay time adjustment is an operation including the operations of the phase comparator S and the delay adjuster 10. The control signal CS is a signal resulting from the operations of the phase comparator 8 and the delay adjuster 10. Therefore, the operations of the phase comparator B and the delay adjuster 10 have been completed at the timed when the control signal CS is generated. Thus, the control signal CS cannot be a signal, which indicates a start of the delay time adjustment. Accordingly, the APA neither teaches nor suggests the feature of increasing the delay time in response to a signal, which indicates a start of adjusting the delay time to adjust the phase of the output signal. Therefore, Applicants respectfully request the withdrawal of the rejection of claim 1 under 35 U.S.C. 102.

Claim 2 is dependent upon claim 1. Thus, it is submitted that for at least the reasons mentioned above, claim 2 recited also recites subject matter that is neither taught nor suggested by the APA. Accordingly, Applicants request the withdrawal of the rejection of claim 2 under 35 U.S.C. 102.

Claims 3-8 were rejected under 35 U.S.C. § 102(e) as being anticipated by Lu (U.S. Patent No. 6,100,735). The Examiner takes the position that Lu teaches or suggests all the features recited in claims 3-8. In view of the above clarification of the claimed invention and the following distinctions, Applicants respectfully submit that the features recited in claims 3-8 are neither taught nor suggested by Lu.

Applicant's independent claim 3 recites a delay time adjusting method of adjusting a delay time of an input first periodic signal so that a phase of the input first periodic signal and a phase of an output second periodic signal match each other based on a comparison between phases of the input first periodic signal and the input second periodic signal, the method comprising the step of adjusting the delay time so that, when a phase of a

predetermined rising edge of the output second periodic signal is behind a phase of a predetermined rising edge of the input first periodic signal, the predetermined rising edge of the output second periodic signal matches a rising edge of the input first periodic signal, a phase of the rising edge being behind and nearest to the phase of the predetermined rising edge of the output second periodic signal, wherein the adjusting of the delay is irrespective of the comparison when starting the step of adjusting of the delay.

Claim 4 is directed to a delay time adjusting method of adjusting a delay time of an input first periodic signal so that a phase of the input first periodic signal and a phase of an output second periodic signal match each other based on a comparison between phases of the input first periodic signal and the input second periodic signal, the method comprising, a first step of judging whether a phase of a predetermined rising edge of said output second periodic signal is behind a phase of a first rising edge of the input first periodic signal, and a second step of increasing the delay time to adjust the phase of the output second periodic signal so that, when the phase of the predetermined rising edge is judged to be behind the phase of the first rising edge in said first step, the phase of the predetermined rising edge and a phase of a second rising edge of the input first periodic signal match each other, the second rising edge being one period behind the first rising edge, wherein the steps of judging and delaying are irrespective of the comparison when starting the delay time adjustment.

Applicant's independent claim 5 recites a delay time adjusting circuit for adjusting a delay time of an input signal so that a phase of the input signal and a phase of an output signal match each other between phases based on a comparison of the input signal and said output signal, the circuit comprising, detecting means for detecting a phase difference between the phase of the input signal and the phase of the output signal, and delaying means for increasing a delay time of the phase of the output signal irrespective of the detection of phase difference when starting the delay time adjustment until the phase difference becomes N periods, where N is an integer other than zero.

Claim 6 recites a delay time adjusting circuit for adjusting a delay time of an input first periodic signal so that a phase of the input first periodic signal and a phase of an output second periodic signal match each other based on a comparison between phases of the input first periodic signal and the input second periodic signal, the circuit comprising,

judging means for judging whether a phase of a predetermined rising edge of the output second periodic signal is behind a phase of a predetermined rising edge of the input first periodic signal, and delaying means for adjusting the delay time so that, when the phase of the predetermined rising edge of the output second periodic signal is judged to be behind the phase of the predetermined rising edge of the input first periodic signal by the judging means, the predetermined rising edge of the output second periodic signal matches a rising edge of the input first periodic signal, a phase of the rising edge being behind and nearest to the phase of the predetermined rising edge of the output second periodic signal, wherein the steps of judging and delaying are irrespective of the comparison when starting the delay time adjustment.

Claim 7 is directed to a delay time adjusting circuit for adjusting a delay time of an input first periodic signal so that a phase of the input first periodic signal and a phase of an output second periodic signal match each other based on a comparison between phases of the input first periodic signal and the input second periodic signal, the circuit comprising, delaying means for delaying the input first periodic signal so as to generate the output second periodic signal, phase-detecting means for detecting whether a phase of a predetermined rising edge of the output second periodic signal is behind a phase of a first rising edge of the input first periodic signal; and adjusting means for controlling the delaying means so that, when the phase of the predetermined rising edge is judged to be behind the phase of the first rising edge by the phase-detecting means, the delaying means delays the phase of the output second periodic signal until the phase of the predetermined rising edge and a phase of a second rising edge of the input first periodic signal match each other, the second rising edge being one period behind the first rising edge, wherein the steps of delaying, phase-detecting and adjusting are irrespective of the comparison when starting the delay adjustment.

Lu is directed to a delay time adjusting method that utilizes a coarse DLL and a fine DLL to generate incremental delay adjustments. However, the DLL, as taught by Lu, can only phase compare during a second pulse. In addition, Lu does not teach or suggest a state detection circuit or a state judgment circuit. Therefore, Lu does not teach or suggest ignoring the phase comparison when starting the delay adjustment. As a result, Lu fails to teach or suggest the feature of adjusting the phase output signal irrespective of the

comparison when starting the delay time adjustment. Applicants respectfully submit that claims 3-7 recite features that recite subject matter that is neither taught nor suggested by the applied reference. Therefore, Applicants request the withdrawal of the rejection of claims 3-7 under 35 U.S.C. 102.

Claim 8 is dependent upon claim 7. In view of above clarification of the claimed invention and the distinctions discussed above, it is respectfully submitted that claim 8 also recites subject matter that is neither taught nor suggested b the applied reference. Accordingly, Applicants request the withdrawal of the rejection of claim 8 under 35 U.S.C. 102.

In view of the above remarks, withdrawal of the rejections to claims 1-8 is respectfully requested. It is respectfully submitted that claims 1-8 recite features that clearly and distinctly claims and contain subject matter that is neither taught nor suggested by the applied references. Accordingly, Applicants submit that the application is now in condition for allowance with claims 1-8 contained therein.

Should the Examiner believe anything further is desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact Applicant's undersigned attorney at the telephone number listed below.

In the event this paper is not considered to be timely filed, Applicant respectfully petitions for an appropriate extension of time. The Commissioner is authorized to charge payment for any additional fees, which may be required with respect to this paper to Counsel's Deposit Account 01-2300, referring to client-matter number 100353-00039.

Respectfully submitted,
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